

PLEB 2 Overview

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Abstract

PLEB 2 is a single-board computer which has been designed to provide a flexible platform on which embedded, real-time and operating systems research may be conducted. It is further intended to provide a reference design which will speed the design of ARM based systems.

Project homepage: <http://www.disy.cse.unsw.edu.au/PLEB>

1 Design Overview

PLEB 2 is a single board computer designed to provide a platform on which both academic research and application implementation can be accomplished. It has been based on PLEB. Design documents were drafted in January, 2003 [2].

1.1 CPU Board

PLEB 2 is based on the XScale PXA255 applications processor from Intel. This device provides a high-performance ARMv5TE core running at up to 400MHz, with a large number of internal peripherals including (but not limited to): an LCD controller, UART(s), PCMCIA, memory/DMA controller, AC97, infra-red communications, I2S, I2C, and MMC. See the PXA255 developers manual [1] for further details.

SDRAM and Flash devices are situated on-board (initial devices give 32MB and 8MB respectively). The PXA255, SDRAM and Flash memory constitute the core of the system. In addition to this, a microcontroller is used to supervise the main processor. The microcontroller is used to: provide remote reset, measure power consumption on the system's power supplies, configure some hardware aspects of the board and provide a ready-to-use JTAG interface.

The system is capable of running off a single Li-ION or Li-Polymer battery between 3.3 and 4.2V. An on-board power supply and battery charger can accept a higher voltage (up to 16V DC), which eliminates the need for a battery should it not be required. The power supply is dynamically adjustable in order to perform scaling of the processor's core voltage.

Peripherals connected on-board include a miniature USB connector connected to the USB-client interface of the PXA255, two push-buttons, an IrDA transceiver, and a RS232 port.

PLEB 2 is designed to be adapted via two mechanisms. Two 100-pin connectors allow daughtercards to be stacked above the CPU board. Virtually all useable signals from the PXA255 are exported to these connectors. A scheme

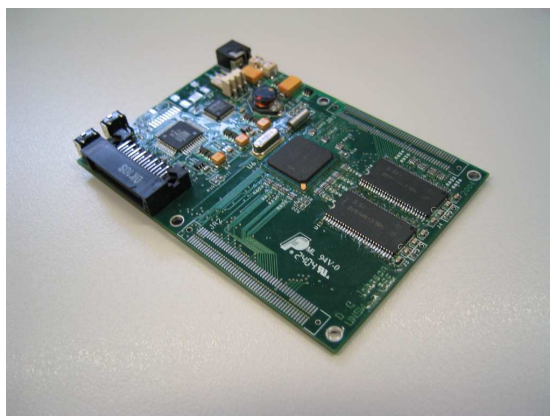


Figure 1: PLEB 2 CPU board

has been developed whereby the CPU can identify which daughtercards are connected and in which order, as well as allocating limited resources (e.g. interrupt request lines, etc). Power can be provided by the daughtercard to the CPU board, as well as from the CPU-board to the daughtercard. The connectors provide an 8mm spacing.

A side-card connector provides access to a small, useful subset of the connections on the daughtercard connectors, as well as the AVR and CPU RS232 ports and direct access to the JTAG lines for an external debugger. This is intended for quick-and-nasty projects, as well as access to the device's serial ports without the use of a daughter card.

The PCB measures 100mm x 70mm (the same dimensions as a 2.5" hard disk drive). Four holes provide for physical mounting.

1.2 Network/IDE/USB Host Board

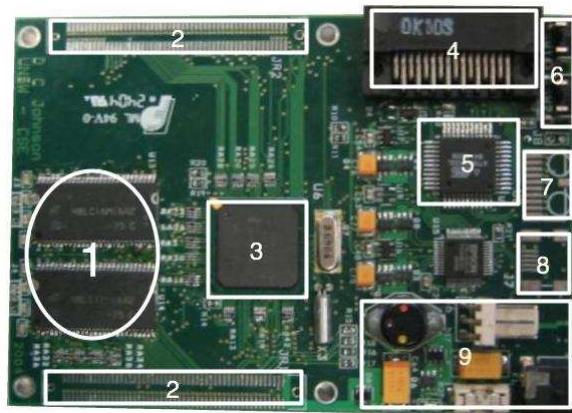
The network/IDE/USB Host board provides access to these three peripherals. The network controller used was a LAN91C111 Non-PCI Ethernet controller. IDE is relatively simple, being interfaced directly to the PXA255's memory bus using a CPLD and some buffering. The USB Host chip is an SL81HS. All three of these peripherals have pre-existing drivers for Linux. Both the LAN91C111 and the IDE drive have drivers in U-Boot.

2 Software support

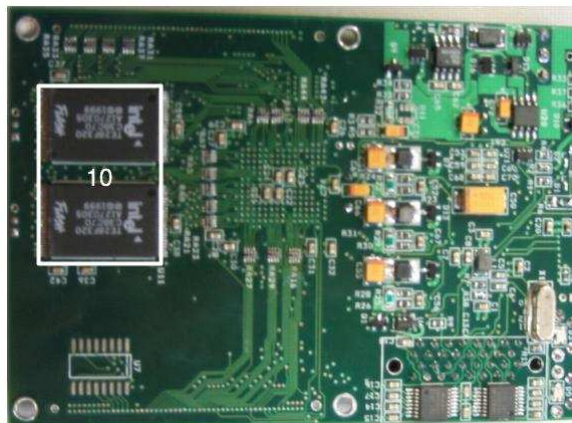
2.1 Bootloader

The U-Boot bootloader was chosen because of its tidy code-base and full feature-set. It was ported to PLEB 2. All basic features work well, including manipulation of and writing to the flash memory. It is suspected that when the Network/IDE/USB Host board becomes available, the bootloader will support booting from the network (via TFTP), and from a hard-disk.

PLEB 2 CPU Top:



PLEB 2 CPU Bottom:



1. SDRAM
2. Daughter card connectors
3. PXA255
4. Side-card connector
5. AVR Mega32 Microcontroller
6. Pushbuttons
7. Infra-red communications
8. USB Client (USB Mini-B)
9. External power supply circuit
10. Flash

Figure 2: PLEB 2 CPU board description

U-boot supports the passing of kernel parameters to Linux, along with the storage of an initial ram-disk.

Boot parameters are stored in flash memory and can be re-written by the bootloader.

Changes necessary to support booting on PLEB 2 have been submitted back to the maintainer, and are available on the PLEB web site [3].

2.2 Operating system

Linux 2.4.19-rmk7-pxa2 has been modified to run on PLEB 2, along with the procurement of an appropriate root disk image. Patches and disk images are available on the PLEB web site [3].

Linux 2.6.10 has also been modified to run on PLEB 2.

A port of L4Ka::Pistachio to the PLEB 2 platform has been completed. Iguana and Wombat support is in progress.

3 Project Status

Goals completed:

- Design, build and test PLEB 2 CPU board
- Write initial microcontroller firmware
- Port U-Boot bootloader to PLEB 2
- Port Linux 2.4 and 2.6 to PLEB 2
- Design Network/IDE/USB Master daughtercard
- Port L4 to PLEB 2

Goals to complete:

- Build and test Network/IDE/USB Master daughtercard (add support to bootloader/Linux)
- Complete microcontroller firmware.
- Develop further peripheral daughtercards.
- Port Iguana and Wombat.

References

- [1] Intel Corporation. Intel PXA250 and PXA210 applications processors, developer's manual, February 2002.
- [2] David Snowdon. PLEB 2: a portable linux embedded box, January 2003.
- [3] David Snowdon. PLEB web site. <http://www.disy.cse.unsw.edu.au/PLEB>, September 2004.